These are sample MCQs to indicate pattern, may or may not appeared in examination

UNIVERSITY OF MUMBAI

Examination 2020 under cluster 9 (FAMT)

Program: BE Computer Engineering

Curriculum Scheme: Revised 2012

Examination: Third Year Semester V

Course Code:CPC501 and Course Name:Microprocessor

Time: 1hour Max. Marks: 50

Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	The number of address and data lines of 8086____ and_____.
Option A:	8 and 8
Option B:	8 and 16
Option C:	16 and 20
Option D:	20 and 16

Q2.	SPARC processor developed by
Option A:	Apple
Option B:	Sun Microsystem
Option C:	Intel
Option D:	Microsoft

Q3.	The flag that acts as Borrow flag in the instruction, SBB is
Option A:	direction flag
Option B:	carry flag
Option C:	parity flag
Option D:	trap flag

Q4.	Which instruction is used to transfer content of BX register into AX
Option A:	MOV AX,BX
Option B:	MOV BX,AX
Option C:	MOV AX,[BX]
Option D:	MOV BX,[AX]

Q5.	If segment address = 1000 H, offset address = 1234 H, then the physical address is----------.
Option A:	11234 H
Option B:	2234H
Option C:	13340H
Option D:	0234H
Q6.	Which of the following is not a data copy/transfer instruction?
Option A:	MOV
Option B:	PUSH
Option C:	DAS
Option D:	POP

Q7.	Which unit in 80386 DX architecture plays a crucial role in the conversion of linear address to physical address?
Option A:	Execution
Option B:	Protection
Option C:	Segmentation
Option D:	Paging

Q8.	In 8086 microprocessor the following has the highest priority among all type interrupts.

Option A:	NMI
Option B:	DIV 0
Option C:	TYPE 255
Option D:	OVER FLOW

Q9.	The data is updated only in the cache and updated at later time in memory is called
Option A:	write through
Option B:	write back
Option C:	write allocation
Option D:	write around

Q10.	What will be the contents of register AL after the following has been executed
	MOV BL,98
	MOV AL,42
	ADD AL, BL
	DAA

Option A:	40 and carry flag is set
Option B:	40 and carry flag is reset
Option C:	DA and carry flag is set
Option D:	DA and carry flag is reset

Q11.	The intel 8086 Microprocessor is a _____ processor
Option A:	8 bit
Option B:	16 bit
Option C:	32 bit
Option D:	4 bit

Q12.	What is the size of segment selector in 80386DX microprocessor?
Option A:	16 bit
Option B:	32 bit
Option C:	48 bit
Option D:	64 bit

Q13.	How many integer pipeline stages are there in Pentium?
Option A:	2
Option B:	3
Option C:	4
Option D:	5

Q14.	_____ is the most important segment and it contains the actual assembly language instructions to be executed by the microprocessor.
Option A:	Data segment
Option B:	Code segment
Option C:	Stack segment
Option D:	Extra segment

Q15.	IN 8259, the register that stores all the interrupt requests in it in order to serve them one by one on a priority basis is
Option A:	Interrupt Request Register
Option B:	In-Service Register
Option C:	Priority resolver
Option D:	Interrupt Mask Register

Q16.	The 80386 DX is…….bit microprocessor.
Option A:	16
Option B:	24
Option C:	8
Option D:	32

Q17.	SPARC stands for
Option A:	Scalable Processor Architecture
Option B:	Super processor Architecture
Option C:	Sun processor architecture
Option D:	Storage Processor architecture

Q18.	How many address lines are required to interface 16 KB memory
Option A:	12
Option B:	16
Option C:	14
Option D:	15

Q19.	The bus is available when the DMA controller receives the signal
Option A:	HRQ
Option B:	HLDA
Option C:	DACK
Option D:	DRQ

Q20.	In mode 2 of I/O mode, which of the following ports are capable of transferring the data in both the directions?
Option A:	PORT A
Option B:	PORT B
Option C:	PORT C
Option D:	PORT D

Q21.	In 8253, the generation of square wave is possible in the mode
Option A:	Mode 1
Option B:	Mode 2
Option C:	Mode 3
Option D:	Mode 4

Q22.	If $\overline{MN/MX}$ is high the 8086 operates in _____ mode.
Option A:	Minimum Mode
Option B:	Maximum Mode
Option C:	Both a and b
Option D:	Medium Mode
Q23.	80386DX is available in a grid array package of
Option A:	64 pin
Option B:	128 pin
Option C:	132 pin
Option D:	142 pin

Q24.	Pentium has following pipelines.

Option A:	AB
Option B:	XY
Option C:	PQ
Option D:	UV

Q25.	All functions of 8255 ports are achieved by programming the bits of internal register called
Option A:	Data bus control
Option B:	Read logic control
Option C:	Control word
Option D:	Write logic